REMARKS

I. Introduction

In response to the Office Action dated June 12, 2007, Applicants have amended claims 1, 5, 9 and 13 in order to further clarify the present invention. Support for the amendment may be found, for example, on page 14, line 21 - page 15, line 11 of Specification, Figs. 1C and 1D; page 18, line 3 - page 19, line 2 of Specification, Figs. 2B and 2C; and page 22, line 23- page 24, line 11 of Specification, Figs. 4B, 4C and 5A. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1, 2, 5, 7, 9 And 11 Under 35 U.S.C. § 102

Claims 1, 2, 5, 7, 9 and 11 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yu (USP No. 6,521,502). Applicants respectfully submit that Yu fails to anticipate the pending claims for at least the following reasons.

With regard to the present invention, amended claims 1, 5 and 9 each recite, in-part, a method for manufacturing a semiconductor device that comprises the successive steps of: (a) forming an amorphous layer; (b) heat treating the amorphous layer, thereby shallowing the depth of the amorphous layer; and (c) after the heat treating step, introducing ions into the heat-treated amorphous layer.

As a result of this process, the present invention maintains the defects that are generated during formation of the amorphous layer at a deep depth of the substrate (the first depth) while by heat treating the amorphous layer, shallows the depth of the amorphous layer to the second depth that is shallower than the first depth. After that, ions are introduced into the heat-treated

amorphous layer, thereby the source/drain impurity layers can be formed without any influence of the defects existing at the first depth. Thus, transistors are not influenced by the defects, and hence, leakage current is suppressed and the crystal structure of the amorphous layer in a region from the first depth to a second depth is restored (see page 19, line 20-page 20, line 5 of Specification).

In contrast to the present invention, Yu fails to recite the order of steps disclosed above. Yu discloses a method for manufacturing a semiconductor device, comprising the steps of: forming an amorphous layer, forming impurity layers (e.g., extension layers 40 and 42, source/drain regions 17, 19, 54 and 56, halo regions 24, 50 and 52), and then heat treating, in that order. As can be seen, the process sequence of Yu is different form that of the present invention.

As a result, Yu fails to disclose that the defects which affect leakage current of the transistors are generated at the interface between the amorphous layer and the crystal (silicon substrate) layer during formation of the amorphous layer. Therefore, in Yu, the impurity layers are formed just after the amorphous layer is formed. Further, as shown in Fig. 1 of Yu, each of the source/drain layers 17 and 19 has the same depth as the amorphous layer 25.

Then, the heat treatment of Yu is performed after the amorphous layer and the impurity layers are formed. This treatment is performed to activate the impurity layers (see column 6, lines 41-45), and changes the amorphous layer from an amorphous state to a single crystalline state (see, column 6, lines 46-48). Thus, the annealing process disclosed in Yu is different from that of the present invention, which is performed in order to shallow the amorphous layer before forming the impurity layers. As such, the Yu method would not prevent the occurrence of the defects affecting the properties of the transistors.

Anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently in a prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986). At a minimum, Yu does not disclose a method for manufacturing a semiconductor device that comprises the successive steps of: (a) forming an amorphous layer; (b) heat treating the amorphous layer, thereby shallowing the depth of the amorphous layer; and (c) after heat treating step, introducing ions into the heat-treated amorphous layer. Therefore, as it is apparent from the foregoing that Yu fails to anticipate amended claims 1, 5 and 9 or any dependent claims thereon, Applicants respectfully request that the § 102 rejection be traversed.

III. The Rejection Of Claims 13, 14 and 16 Under 35 U.S.C. § 103

Claims 13, 14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu (USP No. 6,521,502) in view of Atsuki (US 2002/0069407). Applicants respectfully traverse this rejection of the pending claims for at least the following reasons.

As shown above, amended claim 13 of the present invention also recites a method for manufacturing a semiconductor device that comprises the successive steps of: (a) forming an amorphous layer; (b) by heat treating the amorphous layer, shallowing the depth of the amorphous layer; and (c) introducing ions into the heat-treated amorphous layer.

As it has been shown above that Yu does not teach the same order of the above cited steps, and that the difference in order of steps results in unexpected and superior results, and as Atsuki is not relied upon to remedy this deficiency, the combination of Yu and Atsuki does not render claim 13 obvious. Accordingly, Applicants respectfully request that the § 103 rejection of claim 13 be withdrawn.

IV. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 1, 5, 9 and 13 are patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

V. Conclusion

Having responded to all open issues set forth in the Office Action, it is respectfully submitted that all claims are in condition for allowance.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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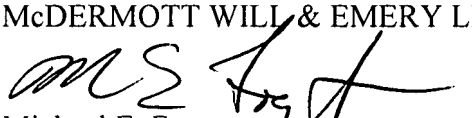

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